Baseband Delay Line (64 µs)

Application

In TV sets the integrated baseband delay line circuit is suitable for decoders with colour difference signal outputs

Description

The integrated Delay Line circuit U3661M is suitable for all chroma decoders with baseband colour–difference outputs. It is suitable for PAL–, SECAM– and NTSC–signals as well. The U3661M contains two separate delay lines for processing (R–Y)–output and (B–Y)–output separately. The delay is performed by internal switched capacitors. On–chip postfiltering avoids the need for external filter components.

A summing circuitry combines the information of adjacent TV–Lines, thus giving an interpolated sum for the PAL–System, storing preceeding lines for the SECAM–System and providing a comb–filtered output for NTSC–Signals. Due to internally generated timing, synchronization is easily done by feeding a line frequent impulse (usually the SSC–Impulse) to the sync–input of the IC.

Features

- One line delay time, addition of delayed and non–delayed output signals
- Adjustment–free application, VCO without external components
- Handles negative or positive colour–difference input signals
- Clamping of AC–coupled input signals [±(R–Y) and ±(B–Y)]
- Line–locked by the sandcastle pulse
- No crosstalk between SECAM colour carriers (diaphoty)
- Comb filtering functions for NTSC colour–difference signals
- Correction of phase errors in the PAL System

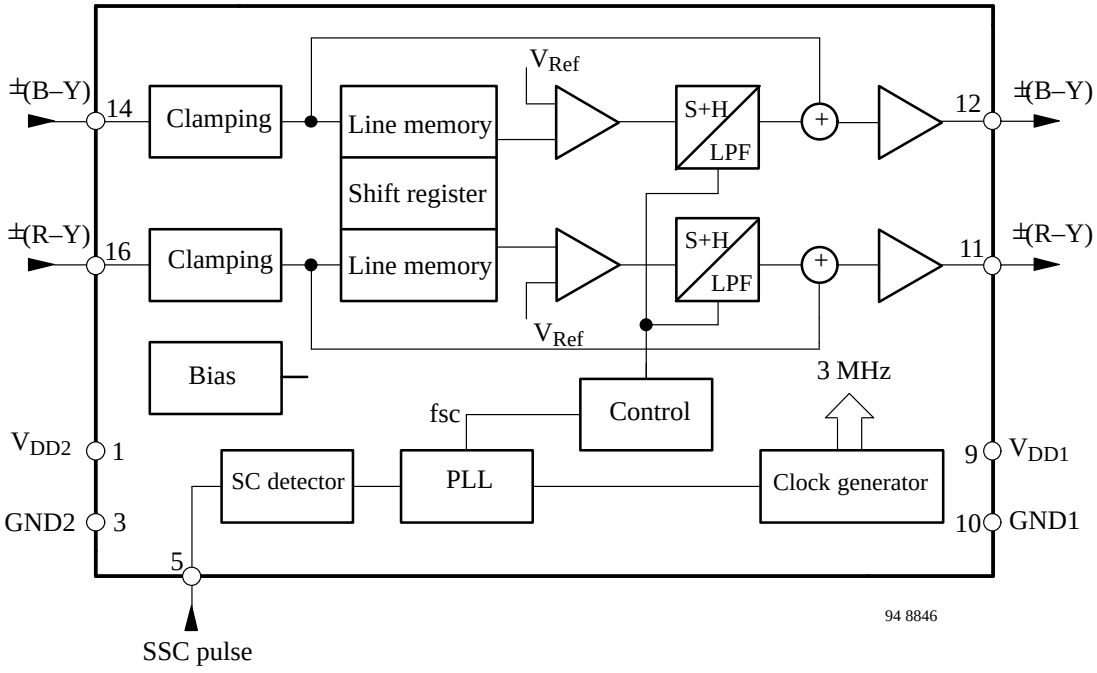


Figure 1. Block diagram

Pin Description

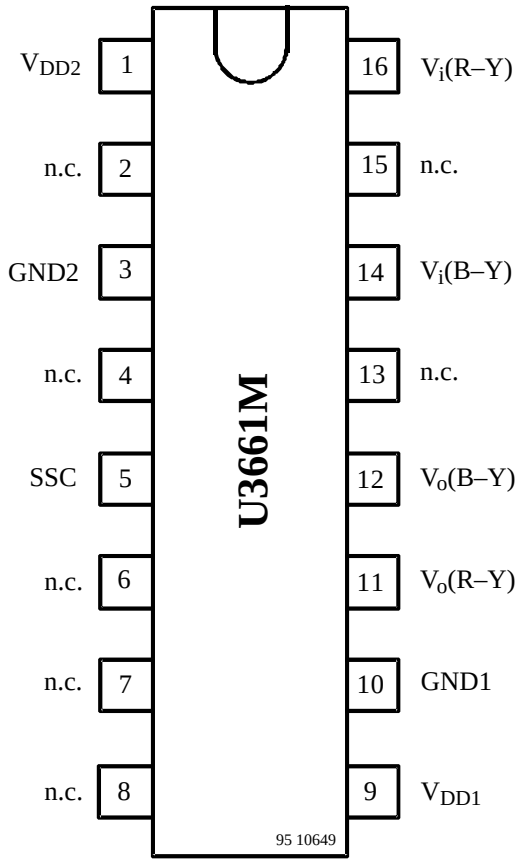


Figure 2. Connection diagram

Pin	Symbol	Function
1	V_{DD2}	Supply voltage for digital part
2	n.c	Not connected
3	GND2	Ground for digital part
4	n.c	Not connected
5	SCC	Sandcastle pulse input
6	n.c	Not connected
7	n.c	Not connected
8	n.c	Not connected
9	V_{DD1}	Supply voltage for analog part
10	GND1	Ground for analog part
11	$V_{o\ (R–Y)}$	± (R–Y) output signal
12	$V_{o\ (B–Y)}$	± (B–Y) output signal
13	n.c.	Not connected
14	$V_{i\ (B–Y)}$	± (B–Y) input signal
15	n.c	Not connected
16	$V_{i\ (R–Y)}$	± (R–Y) input signal

Absolute Maximum Ratings

Reference point Pin 3, 10, unless otherweise specified

Parameters	Symbol	Min.	Typ.	Max.	Unit
Supply voltage (Pin 9)	V_{DD1}	–0.5		+7	V
Supply voltage (Pin 1)	V_{DD2}	–0.5		+7	V
Voltage on Pins 5, 11, 12, 14 and 16	V_n	–0.5		V_S	V
Output current, Pin 11, Pin 12	I_{out}			20	mA
Power dissipation	P			1.1	W
Storage temperature range	T_{stg}	–25		+150	°C
Electrostatic protection* for input/output pins				500	V

* MIL standard 883D, method 3015.7 machine model (all power pins connected together)

Operating Range

Parameters	Symbol	Value	Unit
Supply voltage range (Pin 1, Pin 9)	V_s	4.5 to 5.5	V
Ambient temperature range	T_{amb}	–10 to +70	°C

Thermal Resistance

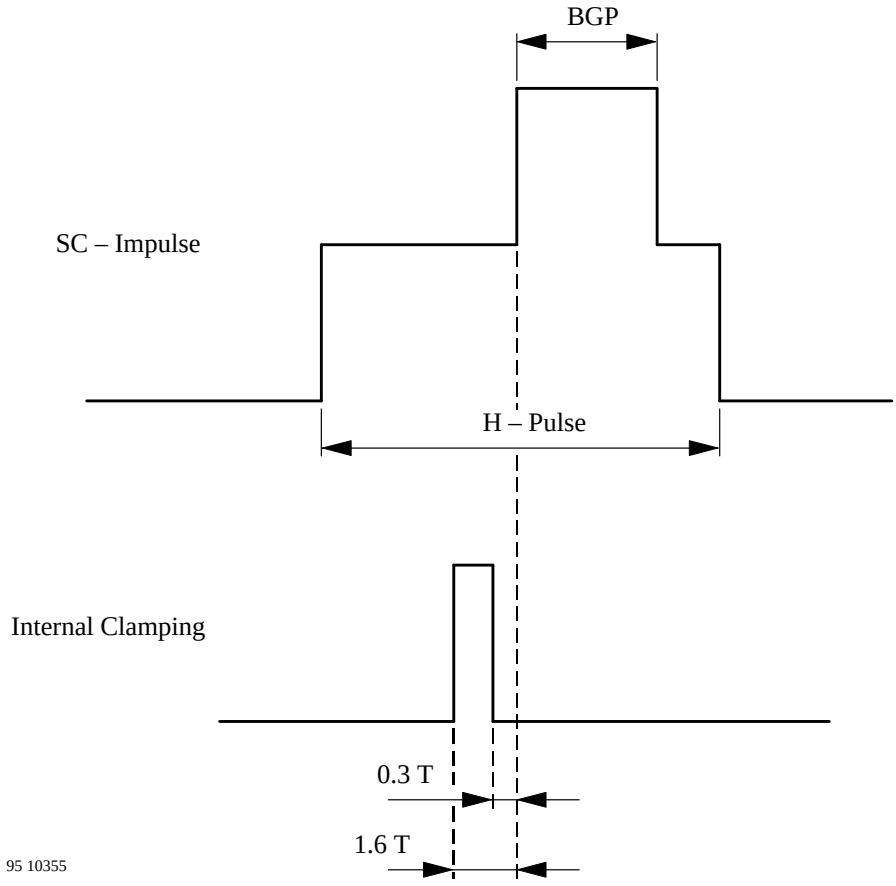
Parameters	Symbol	Value	Unit
Junction to ambient	R_{thJA}	80	K/W

Electrical Characteristics

V_{DD} = 5.0V, T_{amb} = +25°C, reference point ,Pin 3 and Pin 10 connected together, super–sandcastle frequency of 15.625 kHz; unless otherwise specified.

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
DC–supply	**Pin 1, 9**					
Supply voltage (analog part)	Pin 9	V_{DD1}	4.5	5.0	5.5	V
Supply voltage (digital part)	Pin 1	V_{DD2}	4.5	5.0	5.5	V
Supply current (analog part)	Pin 9	I_{S1}		3.5	8.0	mA
Supply current (digital part)	Pin 1	I_{S2}		1	2	mA
Power dissipation		P		30	60	mW
Colour–difference input signals	**Pin 14, 16**					
Input signal (peak–to–peak value)						
±(R–Y) PAL and NTSC	Pin 16	V_i		0.525	1.0	V
±(B–Y) PAL and NTSC	Pin 14	V_i		0.665	1.0	V
±(R–Y) SECAM	Pin 16	V_i		1.05	2.0	V
±(B–Y) SECAM	Pin 14	V_i		1.33	2.0	V
Input resistance	during clamping	R_{14} R_{16}			40	k
Input capacitance		C_{14} C_{16}			10	pF
Input clamping voltage	non colour input level during clamping	V_{14} V_{16}		1.45		V
Colour–difference output signals	**Pin 11, 12**					
Output signal (peak–to–peak value)						
±(R–Y)	all standards Pin 11	V_o		1.05		V
±(B–Y)	all standards Pin 12	V_o		1.33		V
Ratio of output amplitudes at equal in–put signals		V_{11}/V_{12}	–0.4	0	+0.4	dB
DC output voltage	Pin 11, 12	$V_{11,12}$		3.0		V
Output resistance	Pin 11, 12	$R_{11,12}$			400	
Gain for PAL and NTSC	ratio V_o / V_i	G_v	5.5	6.0	6.5	dB
Gain for SECAM	ratio V_o / V_i	G_v	–1.0	0	+1.0	dB
Ratio of output signals for adjacent time samples at constant input signals	$V_{i\ 14,16}$ = 1.33V_{pp} SECAM signals Pin 11 / Pin 12	V(n) / $V_{(n+1)}$		±0.1		dB

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Noise voltage (RMS value)	$V_{i\ 14,16} = 0$ $R_{gen} < 300$ f = 10 kHz to 1 MHz Pin 11, 12	V_{noise}			1.2	mV
Delay of delayed signals		t_d	63.94	64.0	64.06	µs
Delay of non–delayed signals		t_d		65		ns
Transient time of delayed signal	300 ns transient of SECAM input signal, C_{load} = 22 pF Pin 11, 12	t_{tr}		550		ns
Transient time of non–delayed signal	300 ns transient of SECAM input signal C_{load} = 22 pF Pin 11, 12	t_{tr}		350		ns
Sandcastle pulse input	**Pin 5**					
Sandcastle frequency		f_{SC}	14.0	15.625	17.0	kHz
Top pulse voltage	the leading edge of the burst–key pulse is used for timing	V_5	3		Vs+0.7	V
Internal slicing level		V_{slice}	V_5–2.0	V_5–1.5	V_5–1.0	V
Input current		I_5			10	µA
Input capacitance		C_5			10	pF



To avoid interference with succeeding circuitry, the clamping inside the U3661M–B is performed outside of the BGP section !

Figure 3. Timing of internal clamping

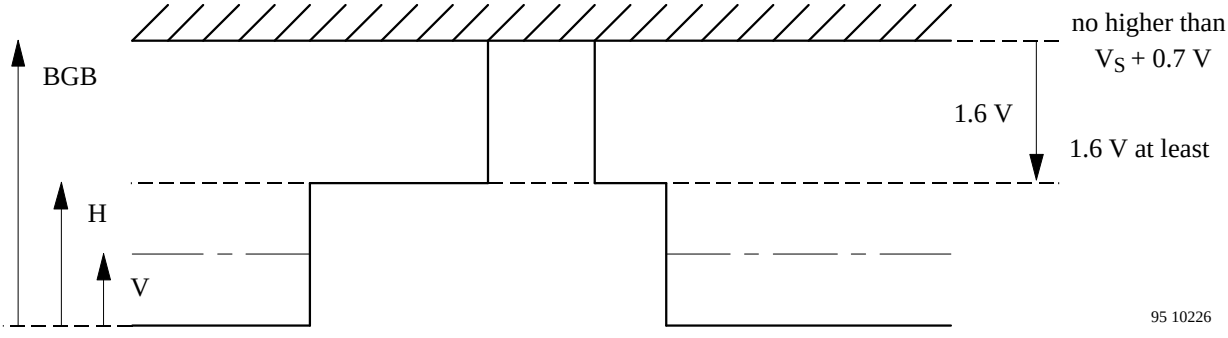


Figure 4. Restrictions to SSC Pulse

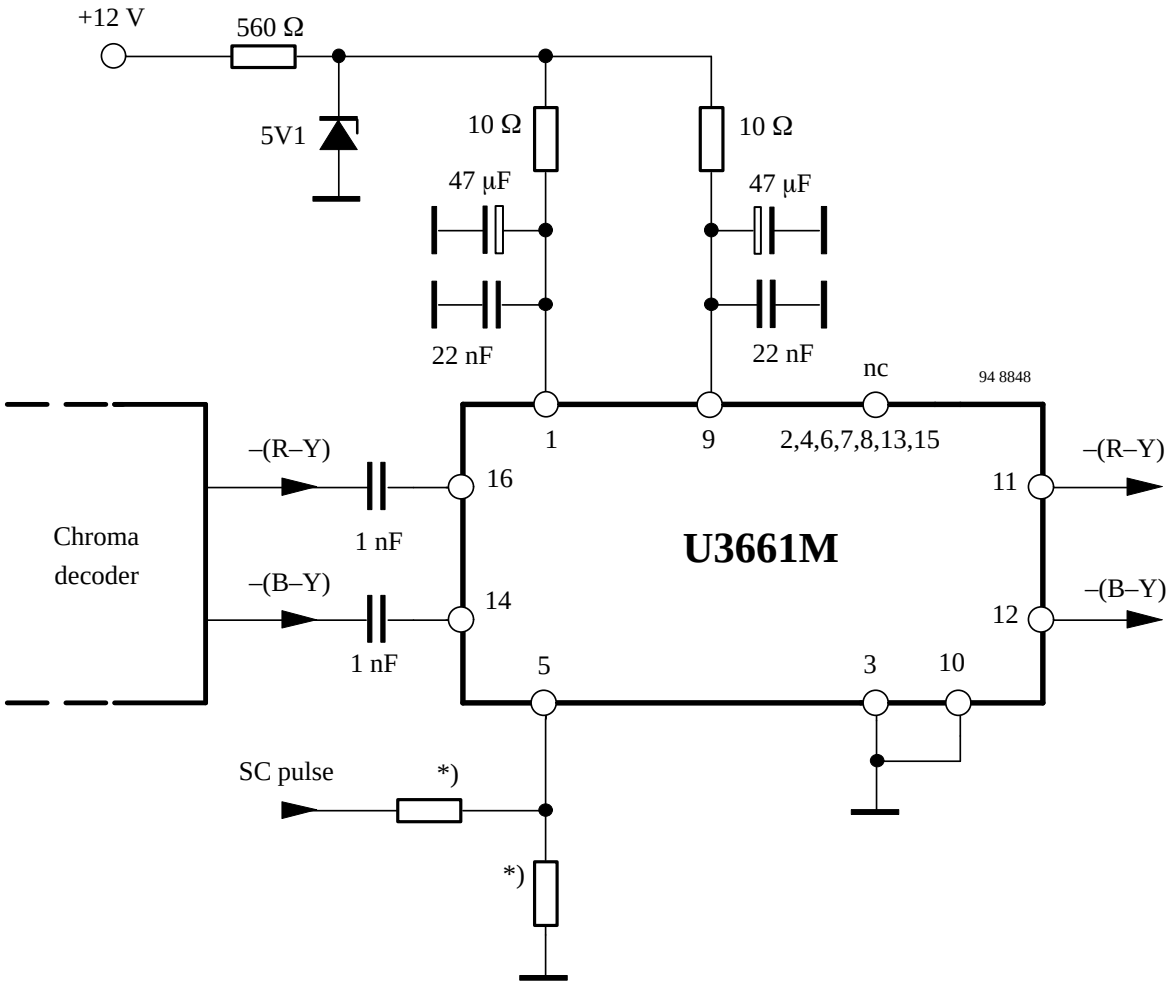


Figure 5. Typical application circuit

*) Application

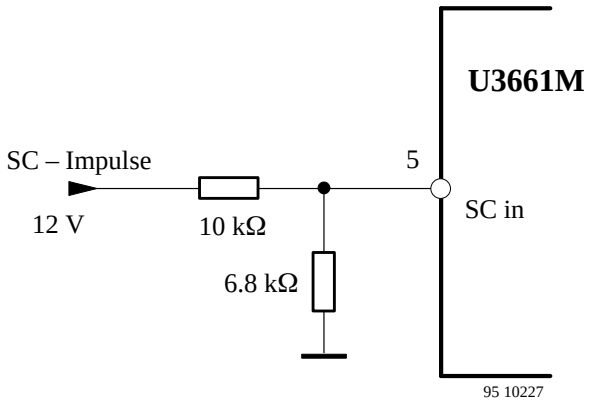


Figure 6. Application with 12 V Sandcastle

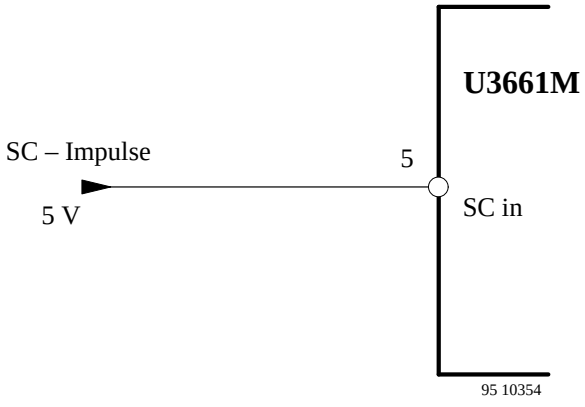


Figure 7. Application with 5 V Sandcastle

Internal Pin Circuits

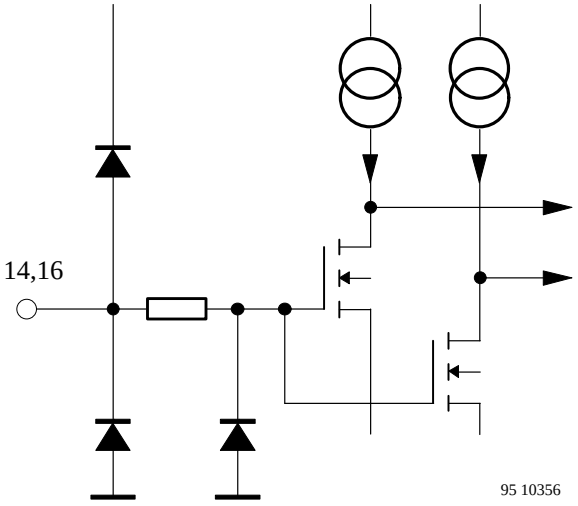


Figure 8. Colour difference signal inputs

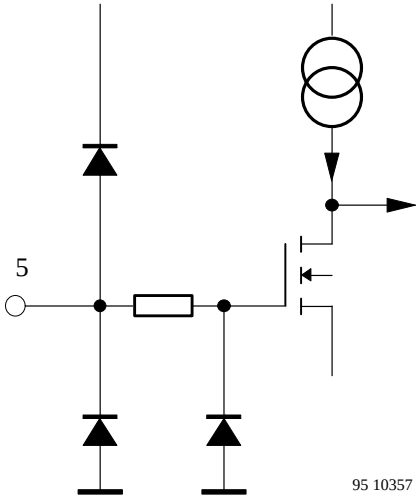


Figure 10. Sandcastle pulse input

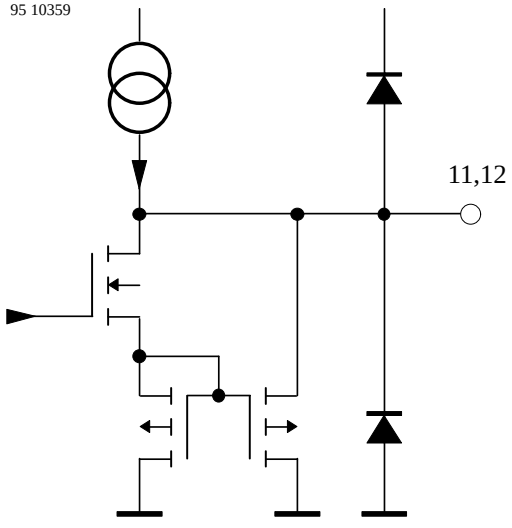


Figure 9. Colour difference signal outputs

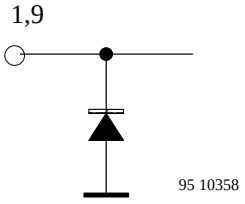


Figure 11. Supply voltage VDD2, VDD1

Ordering Information

Extended Type Number	Package	Remarks
U3661M–ADP	DIP 16	
U3661M–AFP	SO 16	

Package : DIP16
(Dimensions in mm)

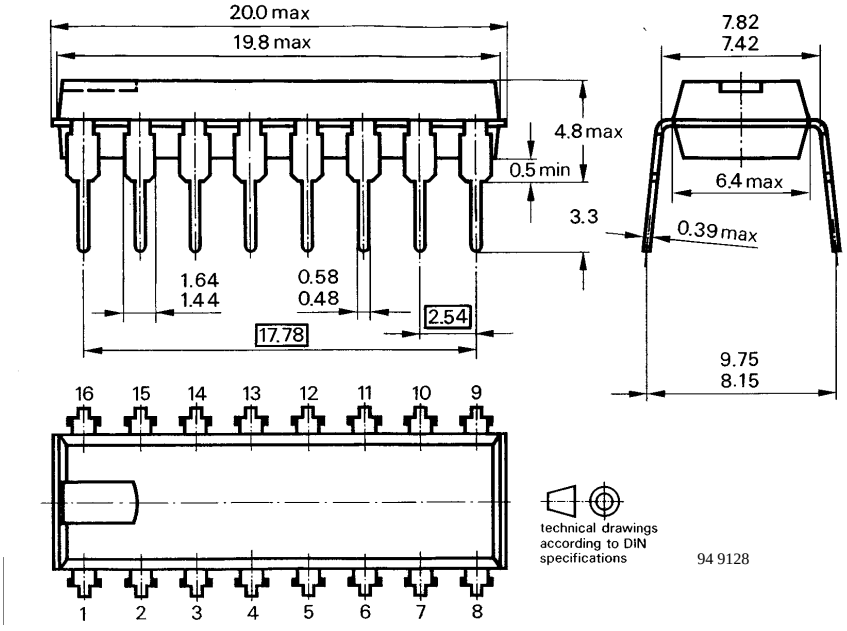


Figure 12. 16 pin dual–inline plastic

Package : SO16
(Dimensions in mm)

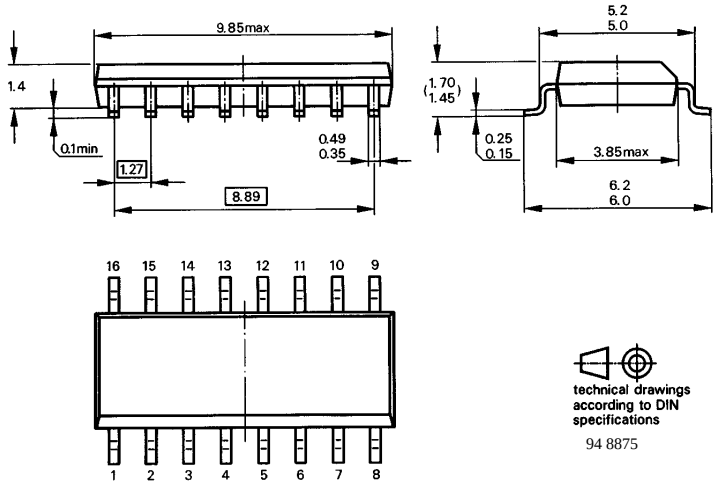


Figure 13. 16 pin SO package

Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC TELEFUNKEN microelectronic GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC TELEFUNKEN microelectronic GmbH semiconductor division has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

TEMIC TELEFUNKEN microelectronic GmbH, P.O.B. 3535, D-74025 Heilbronn, Germany
Telephone: 49 (0)7131 67 2831, Fax number: 49 (0)7131 67 2423